Notice of Allowability	Application No.	Applicant(s)	
	10/649,785	TING ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt filed on 04/10/06*.

2. ☒ The allowed claim(s) is/are *1-7, 8 and 10 (renumbered as 1-9)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

Examiner's statement for reason for allowance

1. Claims **1-8 and 10** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art of record (Applicants' admitted prior art) figure 1 teaches a decoder includes a processor whereby the processor comprising a beta competition block inputs (see figure 5) coupled to a normalizer for normalizing a next step estimates and the output of the estimates coupled back to the processor. The prior art of record, Hepler et al. (U.S. PN: 6,961,921) teach a pipeline architecture for MAP decoder and further. Hepler et al. in figure 3 teach a turbo decoder comprising a calculation stages (24 and 26) calculate alpha and normalize the alpha calculations and each alpha value is calculated on the input register (22) as well as the previously calculated alpha value provided at input (24b) and outputted from calculation stage (26) through multiplexer (28) and register (30), which holds eight calculated values and furthermore the output of register 30 is coupled to the input of alpha memory (32) which stores the first calculated alpha value at the first memory location (32a) and also provides the calculated alpha value to input (24b) (see col. 3, lines 1-23). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a decoder for decoding encoded data, the decoder comprising: a processor having an input which receives probability estimates for a block of symbols, and which is arranged to calculate probability estimates for said symbols in a next iterative state; said calculated probability estimates to provide normalized probability estimates;

a switch arranged to receive both said calculated probability estimates and said normalized probability estimates, output of the switch being coupled to the input of the processor, wherein the switch is arranged to switch state calculated probability estimates and the normalized probability estimates depending on the iterative state. Consequently, claim 1 is allowed over the prior art.

Claims **2-7,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 8:

The prior art of record (Applicants' admitted prior art) figure 1 teaches a decoder includes a processor whereby the processor comprising a beta competition block inputs (see figure 5) coupled to a normalizer for normalizing a next step estimates and the output of the estimates coupled back to the processor. The prior art of record, Hepler et al. (U.S. PN: 6,961,921) teach a pipeline architecture for MAP decoder and further. Hepler et al. in figure 3 teach a turbo decoder comprising a calculation stages (24 and 26) calculate alpha and normalize the alpha calculations and each alpha value is calculated on the input register (22) as well as the previously calculated alpha value provided at input (24b) and outputted from calculation stage (26) through multiplexer (28) and register (30), which holds eight calculated values and furthermore the output of register 30 is coupled to the input of alpha memory (32) which stores the first calculated alpha value at the first memory location (32a) and also provides the calculated alpha value to input (24b) (see col. 3, lines 1-23). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a decoder comprising a processor having an input which receives probability estimates for a block of symbols, and which is arranged to

calculate probability estimates for said symbols in a next iterative state; for normalizing said calculated probability estimates to provide normalized probability estimates, pipelining means between the processor and the normalization means for providing ' non-normalized probability estimates and normalizing means coupled to the processor switching means for receiving both said calculated probability estimates and said normalized probability estimates an output of the switching means being coupled to the input of the processor wherein the switching means is arranged to switch between the calculated probability estimates and the normalized probability estimates depending on the iterative state. Consequently, claim 8 is allowed over the prior art.

Claim **10,** which is/are directly or indirectly dependent/s of claim 8 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER

EA
Ok to enter
05/17/06

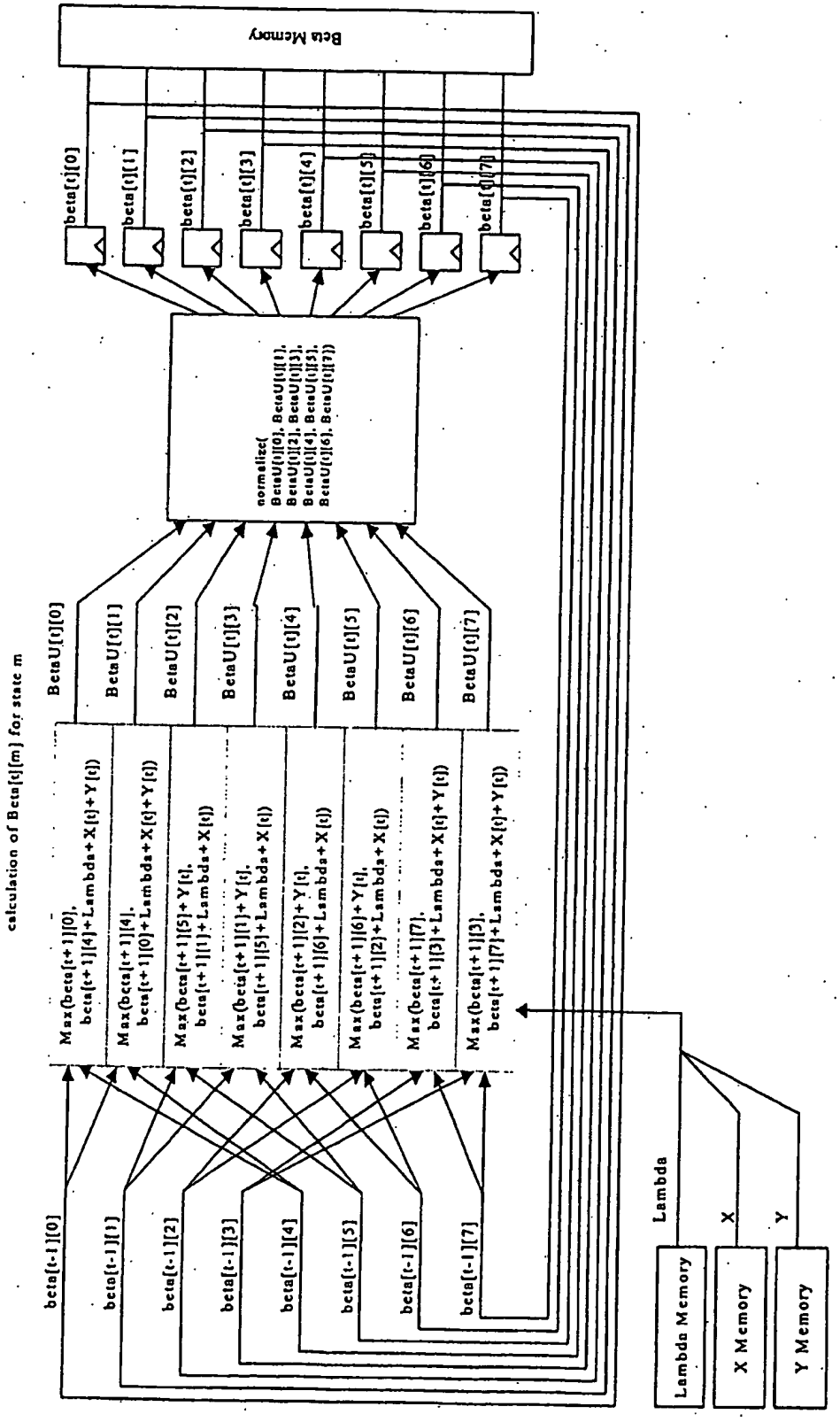

Figure 5. Beta Computation Block Diagram

Prior Art

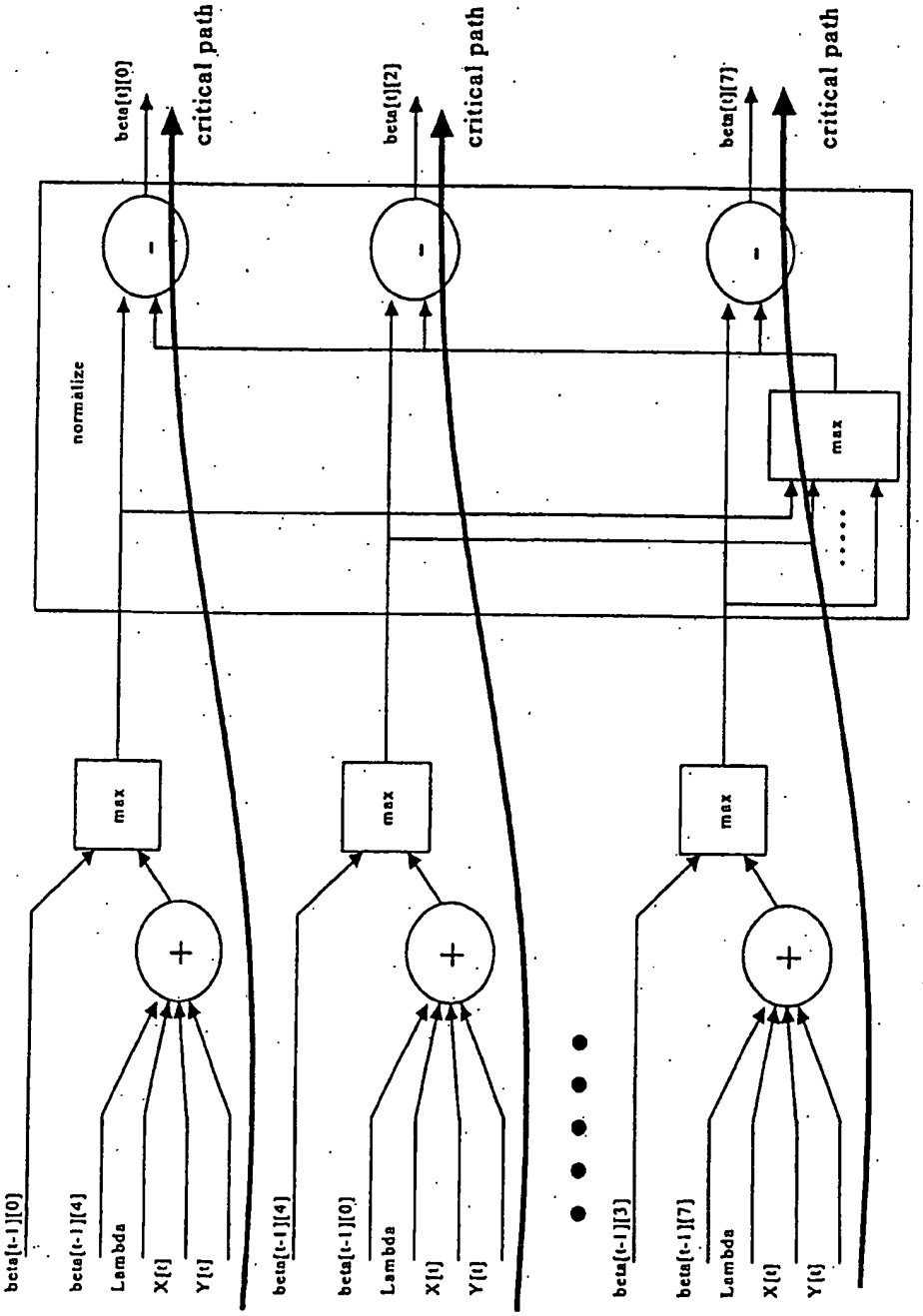

Figure 6 Details Beta Computation and Critical Path Block Diagram

Prior Art

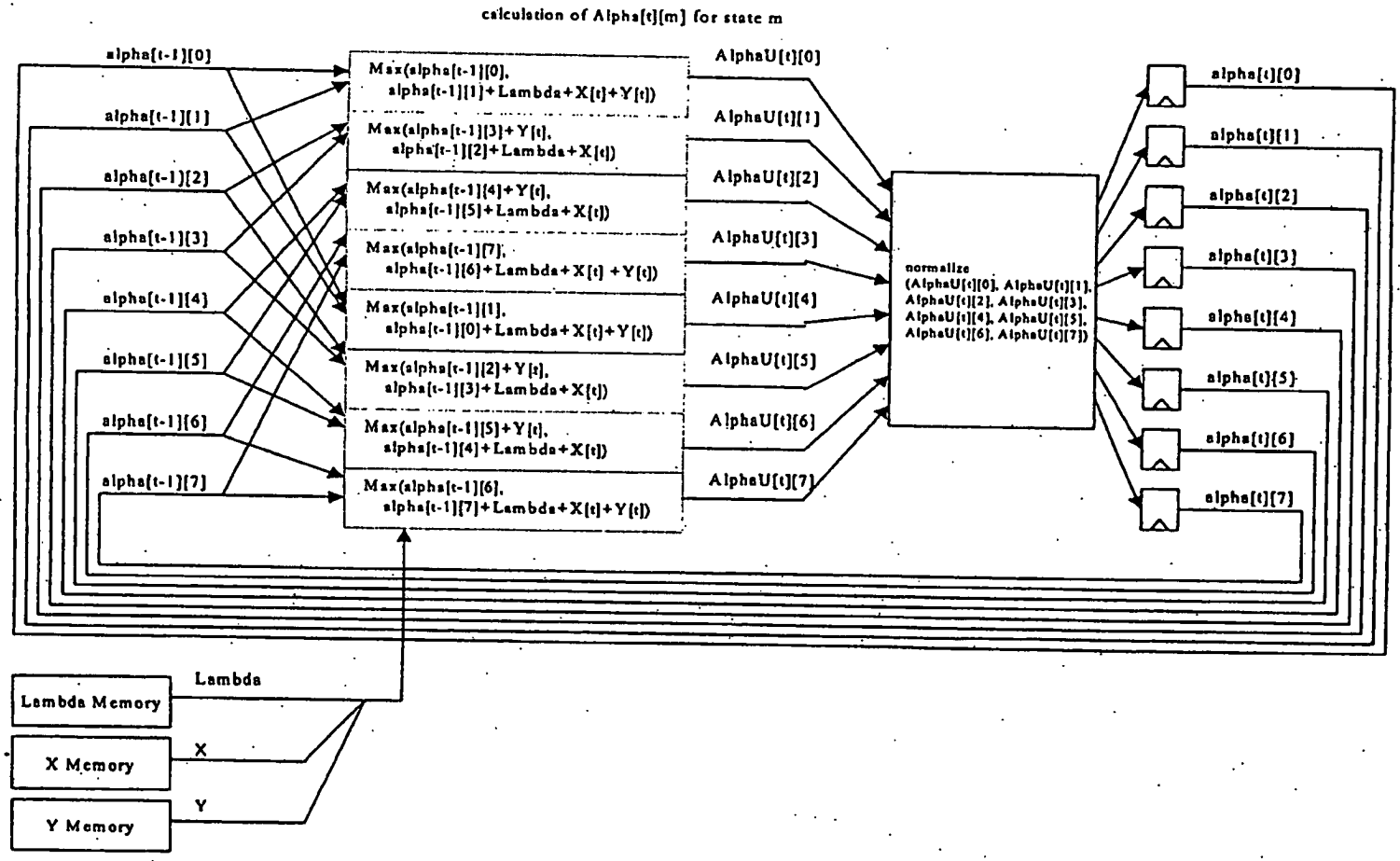

Figure 10 Alpha Computation Block Digram

Prior Art

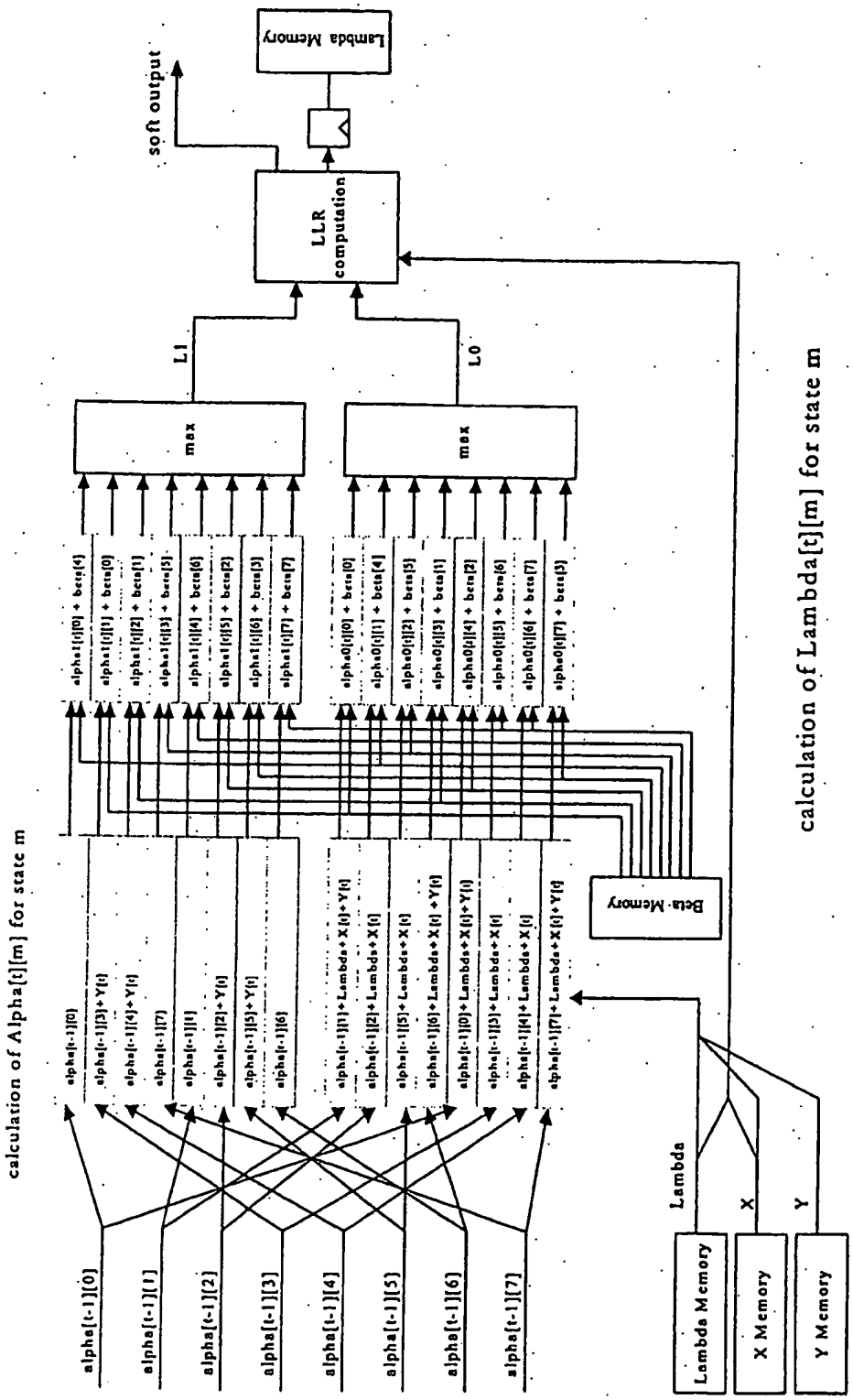

Figure 11 Lambda Computation Block Diagram

Prior Art

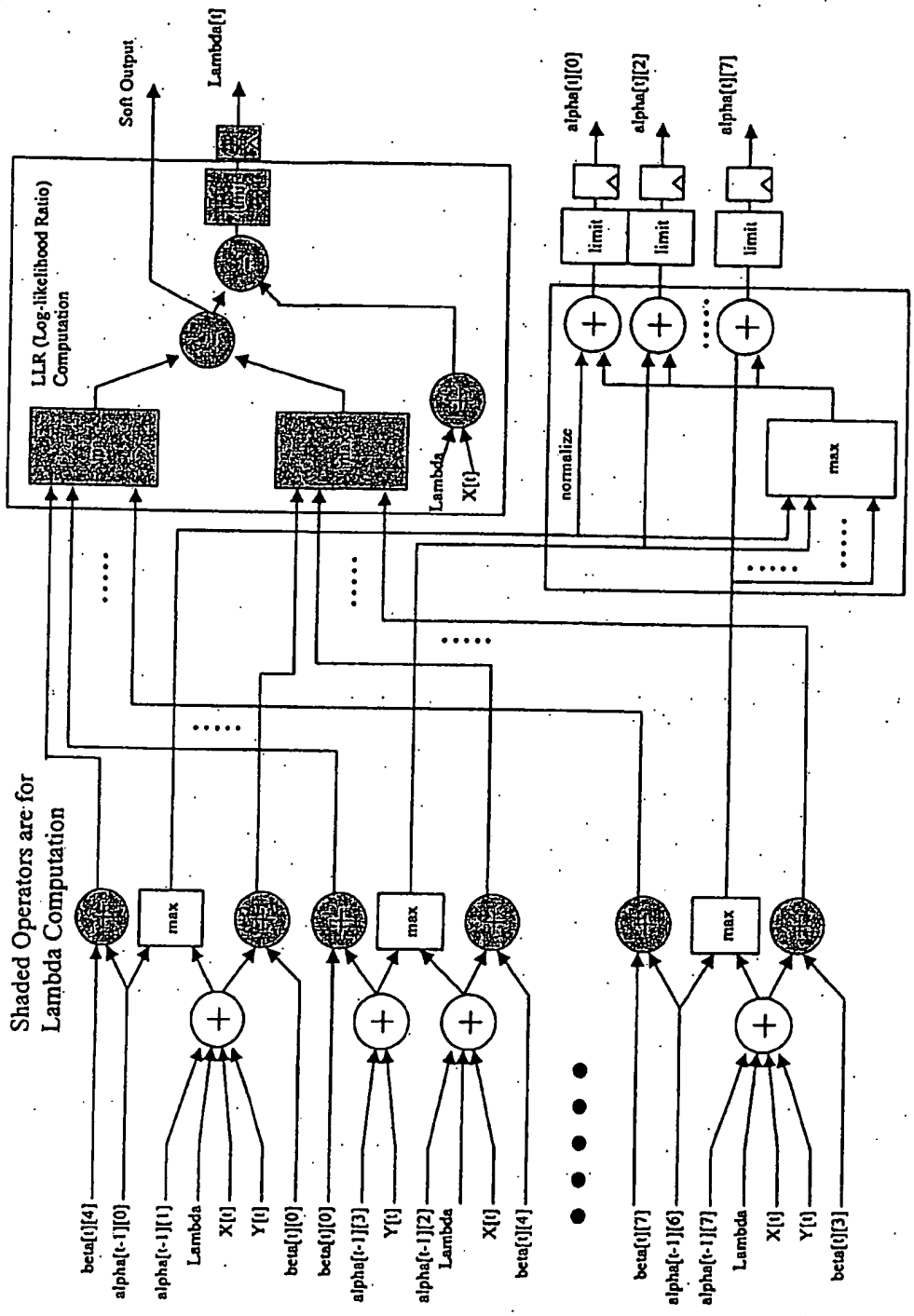

Figure 12 Details Alpha and Lambda Computation and Critical Path Block Diagram

Prior Art